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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,636	09/19/2003	Rebecca A. Kocot	5201-27000 03-0914	5055
Leo Peters LSI Logic Corporation 1621 Barber Lane, MS D-106 Milpitas, CA 95035				
7550	04/06/2009	EXAMINER KANG, INSUN		
ART UNIT		PAPER NUMBER		
2193				
MAIL DATE		DELIVERY MODE		
04/06/2009		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Advisory Action  
Before the Filing of an Appeal Brief**

**Application No.**

10/664,636

**Applicant(s)**

KOCOT, REBECCA A.

**Examiner**

INSUN KANG

**Art Unit**

2193

***--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

THE REPLY FILED 23 March 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☐ The period for reply expires \_\_\_\_\_ months from the mailing date of the final rejection.  
b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.  
Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: 1 and 3-20.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_  
13. ☐ Other: \_\_\_\_\_.

/Insun Kang/  
Examiner, Art Unit 2193

Continuation of 11, does NOT place the application in condition for allowance because:

The applicant states that: 1) Aihara with Stolte do not teach a graphical user interface for receiving user input to select one instruction address nor does the combination teach or suggest a designator to denote that a corresponding designated instruction address will proceed to a succeeding stage in a processor pipeline using a next clock cycle (remark, 2). The applicant further states that Stolte does not teach a pipeline view of many instructions at a particular time can be displayed along with dependencies between instructions in the pipeline view which the user can select or deselect. As such, the cited portions of Stolte do not teach a GUI for receiving user input to select one of the instruction addresses as recited in claim 1. On the contrary, the cited portions of Stolte teach a group of instructions are displayed to which a user can select or deselect a dependency between a pair of instructions. Therefore, the cited portions of Stolte, as applied by the Examiner, do not cure the deficiencies of Aihara (remark, 3). While the cited portions of Aihara may teach a state at which instructions in execution in a pipeline are located at and which stages are stalled, the cited portions of Aihara do not teach or suggest a designator to denote that a corresponding designated instruction will proceed to a succeeding stage in a processor pipeline during a next clock cycle. On the contrary, the cited portions of Aihara only teach what stage in an instruction at, not whether it will proceed to a succeeding stage in the processor pipeline during a next clock cycle. As such, the cited portions of Aihara do not teach a designator to denote that a corresponding designated instruction address will proceed to a succeeding stage in a processor pipeline during a next clock cycle (remark, 4).

In response, the instant invention is directed to visualization of a DSP/superscalar pipeline information obtained from a source code debugger and implemented in conjunction with the cycle-accurate processor modeling simulator. The instant specification states that the "ordering of instructions in the pipeline stages is presented in the context of the developer's code rather than in the context of the pipelining itself (page 10 lines 24-27)." The currently active state is highlighted with a color where the color corresponds to the stage designator (page 16 lines 2-14) in the instant invention. Aihara and Stolte also disclose pipeline visualization systems. Specifically, Aihara clearly discloses a debugger connected to a cycle-accurate instruction set simulator comprising pipeline information displayed on a display screen (i.e. 0022; 0045). The GUI of the source debugger in Aihara displays the pipeline information and the situation of the execution of respective instructions on the pipeline can be thereby grasped adequately via the input device 17 (0044). By using the debugger, it is possible to grasp the current position of the program processing, the progress of processing at the respective stages and the like (0053). The pipeline stage information is stored as to which instruction is in execution at each stage of the pipeline in order to take the pipeline processing into consideration (0045). Aihara also clearly discloses using a color as a designator and non-designator for the stalled and proceeding stages (0057). The screen display of the source code debugger displays the source code on the display device with an arrow in front of an address indicating a current position of execution of the program with pipeline stage signs (0055) displayed in different colors (0057). The stall information storage unit stores information as to whether each stage is in an executable condition or a stalled condition (0045). The storage unit stores information concerning the dependency relations of the registers designated as operands of the respective instructions in progress of processing on the pipeline in order to judge whether the pipeline will stall or not (0045). Aihara states that the "marks indicating stalled stages are highlighted in reverse video or in a different color (0064)" where the stages without the stall mark is highlighted in a different color (designator) from the highlighted color for the stalled stages and will "proceed with the E stage upon execution of the next step (0063)." Therefore, it is clear that the color indicating the stage that will proceed with the E stage upon execution of the next step without being stalled corresponds to the designator in the instant invention. Furthermore, although it is not clearly recited in Aihara that an instruction address in the debugger is selected by a user, Stolte clearly recites a user-controlled pipeline view so that a particular instruction address can be selected by a user to show all instructions in the pipeline at a particular point in time (fig. 2; page 5, left col.) where the user controls enable the user to "single-step" through the pipeline to observe the instruction sequences in the pipeline view (page 5).